



Substitute for form 1449A/PTO				<i>Complete If Known</i>	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	09/977,600
				Filing Date	October 12, 2001
				First Named Inventor	Wolf-Dietrich Weber
				Art Unit	2187 2189
				Examiner Name	Christian Chace
				Attorney Docket Number	2998P018
Sheet	1	of	5		

Examiner Signature	<u>Ant. P. Cen</u>	Date Considered	2/22/06
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials'	Cite No.'	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ¹
CR		"International Search Report", International Searching Authority, August 9, 2005, 9 pages, PCT/US2004/035863.	
CR		"European Search Report", European Patent Office, November 30, 2004, 3 pages, EP 02 70 7854.	
CR		Wingard, Drew, "MicroNetwork-Based Integration for SOCs", Design Automation Conference, June 2001, pp. 673-677.	
CR		Ho, Ron, et al., "The Future of Wires", Proceedings of the IEEE, Vol. 89, No. 4, April 2001, pp. 490-504	
CR		Dally, William J. et al., "Route Packets, Not Wires: On-Chip Interconnection Networks", Design Automation Conference, June 2001, pp. 684-689.	
CR		Kurose, Jim, "Open Issues and Challenges in Providing Quality Service Guarantees in High-Speed Networks", ACM Computer Communication Review, Vol. 23, No. 1, January 1993, pp. 6-15.	
CR		Zhang, Hui, "Service Disciplines for Guaranteed Performance Service in Packet-Switching Networks", Proceedings of the IEEE, Vol. 82, No. 10, October 1995, pp. 1374-1396.	

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CC		Stiliadis, Dimitrios et al., "Latecy-Rate Servers: A General Model for Analysis of Traffic Scheduling Algorithms", In Proceedings of IEEE INFOCOM 96, April 1996, pp. 111-119.	
CC		Lahiri, Kanishka et al., "LOTTERYBUS: A New High-Performance Communication Architecture for System-on-Chip Designs", Design Automation Conference, June 2001, pp. 15-20.	
CC		Dally, William J., "Virtual-Channel Flow Control", In Proceedings of the 17th Int. Symp. on Computer Architecture, ACM SIGARCH, May 1990, Vol. 18, No. 2, pp. 60-68.	
CC		Wingard, Drew, "Integration Architecture for System-on-a-Chip Design", IEEE 1998 Custom Integrated Circuits Conference, May 1998, pp. 85-88.	
CC		Weber, Wolf-Dietrich, "Enabling Reuse via an IP Core-centril Communications Protocol: Open Core Protocol", In Proceedings of the IP 2000 System-on-Chip Conference, March 2000, pp. 1-5	
CC		Adan, Ivo et al., "Queueing Theory", Eindhoven University of Technology, February 14, 2001, pp. 23-27, XP-002329104.	
CC		Wingard, Drew, "Sonics SOC Integration Architecture", Sonics, Inc., 1500 presentation, 1999, 25 pages, www.OCP-IP.org	

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CPC		Kamas, Alan, "The SystemC OCP Models; An Overview of the SystemC Models for the Open Core Protocol", NASCUG, 2004, 30 pages.			
CPC		Wingard, Drew, "Socket-Based Design Using Decoupled Interconnects", Sonics, Inc., 30 pages, downloaded June 14, 2004, www.OCP-IP.org			
CPC		Haverinen, Anssi, "SystemC™ based SoC Communication Modeling for the OCP™ Protocol", White Paper, October 2002, V1.0, 39 pages.			
CPC		Wingard, Drew, "Tiles - An Architectural Abstraction for Platform-Based Design", Perspective article 2, EDA Vision, June 2002, 4 pages, www.edavision.com.			
CPC		Weber, Wolf-Dietrich, "Efficient Shared DRAM Subsystems for SOCs", Sonics Inc., 2001, 6 pages.			
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CPC		Wingard, Drew PhD, "Integrating semiconductor IP using μNetworks", ASIC Design, July 2000 electronic engineering, 3 pages.			

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CH		Wingard, Drew, "Tiles: the Heterogeneous Processing Abstraction for MPSoC", Sonics, Inc., Smart Interconnect IP, 2004, 35 pages, www.OCP-IP.org	
CH		Chou, Joe, "System-Level Design Using OCP Based Transaction-Level Models", presentation, Denali MemCon Taiwan 2005, OCP International Partnership, 23 pages.	
CH		Wingard, Drew, "A Non-Blocking Intelligent Interconnect for AMBA-Connected SoC's", Sonics Inc., CoWare Arm Developer's Conference, October 6, 2005, 39 pages.	
CH		Weber, Wolf-Dietrich et al., "A quality-of-service mechanism for interconnection networks in system-on-chips", 1530-1591/05, 2005 IEEE, 6 pages.	
CH		Casini, Phil, "Measuring the value of third party interconnects", Sonics, Inc., White Paper, 2005, 11 pages, www.sonicsinc.com.	

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